REMARKS

Some claims have been cancelled without prejudice and some of the rejected claims have been amended. No new matter has been added.

Applicants submit this Amendment "D" and Response for the Examiner's consideration. Reconsideration of the application, as amended, in view of the following remarks are respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-43 were presented for examination; claims 1-27, 31-40, and 42-43 stand rejected and pending in the application. Claims 28-30 and 41 have been cancelled without prejudice. The rejections are addressed hereinbelow.

2. RESPONSE TO REJECTIONS AND OBJECTIONS

2.1. *Claim Objections*

Claim 2 has been objected for the reason set forth in the Office Action. Claim 2 recites "A method according to Claim 1, further comprising forming a liner upon a sidewall of each said isolation trench" and it is asserted in the Office Action that "the rounding the top edge of the trench is an inherent result of forming the liner. Thus, claim 2 do[es] [sic] not appear to further limit[] [sic] claim 1." (Underlining in the original). Independent claim 1, from which claim 2 directly depends, recites in part "rounding the top edge of each of said isolation trenches". Applicants traverse the asserted objection for at least the following reason.

The natural result of rounding the edge of a trench is not necessarily the formation of a liner. Whereas the obtention of a rounded edge may result from the formation of a liner, and whereas

rounding an edge may be performed while forming a liner, these conditions are not sufficient to establish inherency. Therefore, the recitation in claim 2 adds a further limitation to claim 1.

Applicants respectfully request the reconsideration and withdrawal of this objection.

2.2. *Claim Rejections Under 35 U.S.C. § 112 ¶ 1*

Claims 1-17, and 42-43 stand rejected under 35 U.S.C. § 112 ¶ 1.

Independent claims 1, 14, and 43, and by incorporation their respective dependent claims, recite "wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench" (claim 1), "wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench." (claim 14), and "wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches" (claim 43).

Independent claim 7, and by incorporation its dependent claims, and independent claim 42 recite "planarizing with a single etch recipe".

The Office Action refers to the foregoing recitations and asserts that they fail to comply with the written description requirement. Applicants cite below, by way of illustration but not as interpretive limitations, instances of support in the Application as filed for these claim recitations.

Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. *See, e.g.*, Application, p. 3, *ll.* 25-26, p. 6, *ll.* 1-3, p. 15, *l.* 4, p. 20, *ll.* 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that

is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing show possession of the claimed invention.

The Application as filed refers in uses in numerous instances terms such as "single etchback step" (while describing that the "topographical reduction of the third dielectric layer may also be carried out as a single etchback step that sequentially removes superficial portions of the third dielectric layer that extend out of the isolation trench.") and "the single etchback uses an etch recipe" (while describing that "[t]he single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first dielectric layer".) *See, e.g.*, Application, p. 6, *ll.* 5, 10. Applicants submit that these illustrative expressions provide support for the use of the terms "single etch recipe" and that they show possession of the claimed invention to a person of ordinary skill in the art.

Applicants respectfully request the reconsideration and withdrawal of this rejection.

2.3. *Claim Rejections Under 35 U.S.C. § 112 ¶ 2*

Pending claims 9, 10, 12-13, and 26-27 stand rejected. Claim 9 recites, *inter alia*, "said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1." Various terms in this recitation are emphasized in the Office Action by italicization or by bold-facing with underlining, and the Office Action asserts that there is insufficient antecedent basis for this limitation in the claim.

If the antecedent basis refers to the italicized terms in the Office Action, Applicants submit that each one of such terms has antecedent basis in independent claim 7 from which claim 9 directly

depends. If the antecedent basis refers to the terms in bold face and underlined in the Office Action, Applicants submit that these terms recite a characteristic of the etch process for which there is written support in the Application, that such characteristic is recited in claim 9 as a limitation, and that such further limitation does not need any additional antecedent basis in independent claim 7.

Dependent claims 10, 12 and 13 depend from dependent claim 9. Claim 27 depends from independent claim 26. With the antecedent recitations from the respective parent claims, the Office Action refers to an etch recipe that etches a first dielectric layer faster than a conformal layer and spacers by a ratio in a range from about p:q to about r:s. (With language variations in the claim recitations, and wherein p, q, r and s represent different numbers recited in the claims). The Office Action selects a portion of the written description and interprets it as if it disclosed what the Office Action characterizes as a complete opposite to what these claims recite.

Applicants respectfully traverse this rejection and submit that the Office Action seems to rely on the adoption of an interpretation of the term "selective" that appears to differ from that introduced by the drafter in the capacity of being his own lexicographer . The steps, operations, and results of the etching processes disclosed in the Application are clearly shown in the specification and accompanying drawings. Therefore, the embodiments of these methods appear clear in light of the ordinary skill in the art. The cites and quotes to the Application as filed provided herein are given for illustrative purposes, but not as interpretive limitations.

The Application as filed provides, for example, that "[t]he single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first isolation trench while removing substantially all remaining portions of the first dielectric layer. The resulting structure can be described as having the shape of a nail." Application, p. 6, *ll.* 8-13. As indicated

in the Office Action, the written description also provides that "planarization will be selective to insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2;1, selective to isolation film 36 as compared to insulator island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly selective to spacer 28 over insulator island 22. Preferably spacer 28 and isolation film 36 are made from the same material such that the etch will be substantially uniform as tot he selectivity thereof with respect to spacer 28 and isolation film 36 over insulator island 22." Application, p. 14, *ll.* 17-25. Various drawings, such as Figs. 6A-8A and 6B-8B, are provided in the Application regarding these operations.

Applicants note that "selectivity", and related terms, in this context convey a meaning of degree rather than a meaning of total exclusion. When a plurality of materials are exposed to the process being referred to, the various selectivity rates apply as described and as illustrated in the drawings. When only one material is exposed to the process being referred to, such as isolation film 36 in Fig. 6A, then this material is gradually removed to form the structures shown in Fig. 7A. This interpretation follows from the specification and drawings, and the meaning of terms used in the claims and in the written description as understood in the art. Furthermore, there is no contradiction between the recitation in the pending claims and the description provided in the various parts of the Application as filed.

Applicants respectfully request the reconsideration and withdrawal of this rejection.

2.4. *Claim Rejections Under 35 U.S.C. § 102(b)*

Claims 1-4, 6-7, 11, 38, and 41 stand rejected in light of Omid-Zohoor, *et al.*, U.S. Pat. No. 6,184,108 (hereinafter "the '108 patent ") and claim 43 stands rejected in light of Omid-Zohoor, U.S. Pat. No. 6,097,072 (hereinafter "the '072 patent ").

Independent claims 1 and 7 recite, *inter alia*, "forming a second dielectric layer over said oxide layer and said first dielectric layer " and "wherein each said spacer is situated upon said oxide layer". These recitations are incorporated in the rejected claims that depend from claims 1 and 7. To further clarify these recitations, claims 1 and 7 have been amended to recite "wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas ". Support for this amendment is found, for example, in the quoted original claim language itself, Figs. 4A-4B and p. 11.

In contrast, the '108 patent discloses an oxide etch to remove the portions of pad oxide layer 42 that are exposed at regions 48, as shown in Fig. 3D therein, and to subsequently deposit spacer oxide layer 50 over the exposed semiconductor substrate 40 at regions 48, as shown in Fig. 3E therein. *See also*, the '108 patent, col. 4, *ll.* 3-8. Furthermore, Fig. 3F in the '108 patent shows the formation of sidewall spacers 52 at the sides within exposed regions 48 and at the sides of the terminal portions of pad oxide layer 42 therein. Even if Fig. 3F in the '108 patent did not show the formation of spacers 52 as indicated, such spacers in the '108 patent cannot be situated upon pad oxide layer 42 because spacers 52 are formed within exposed regions 48 and it is precisely within these regions that pad oxide layer 42 been removed by an oxide etch as indicated above. Therefore, even if, *arguendo*, the layers disclosed in the '108 patent could be analogized with those recited in the rejected claims, the present claims are not anticipated by the '108 patent.

Independent claim 38 recites, *inter alia*, "having a spacer ... upon said oxide layer in contact with said first layer" and "wherein said filling is performed by depositing said second layer and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer". *See, e.g.*, Application, p. 13, *ll.* 22-24, p. 18, *ll.* 25-26, p. 19, *l.* 1. In contrast, the '108 patent discloses a spacer that is not upon any oxide layer, but that it is instead directly on top of semiconductor substrate 40. Furthermore, the '108 patent discloses the formation of a layer within gap 60 that is required not to fill such gap to be able to accommodate a subsequent oxidative process. Therefore, even if, *arguendo*, the layers disclosed in the '108 patent could be analogized with those recited in the rejected claim, the present claim is not anticipated by the '108 patent.

Claim 43 recites at least one of the following features: forming at least one isolation trench that has a rounded top edge; planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, none of at least these features is disclosed in the '072 patent.

Because of at least the foregoing recited features, the cited patents do not disclose each and every step of the methods recited in the rejected claims. Consequently, the cited patent do not anticipate the methods recited in these claims. Applicants respectfully submit that the pending claims patentably distinguish over the cited patents, and reconsideration and withdrawal of this rejection is respectfully requested.

2.5. ***Claim Rejections Under 35 U.S.C. § 103(a)***

Claims 5 (dependent from independent claim 1), 8 (dependent from independent claim 7), independent claim 14 and its dependent claims 15-17, independent claim 35 and its dependent claims

36-37, and claims 39-40 (dependent from independent claim 38) stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of the '108 patent and at least one of the '072 patent, Poon, *et al.*, U.S. Pat. No. 5,387,540 (hereinafter "Poon"), and Lee, *et al.*, U.S. Pat. No. 5,229,316 (hereinafter "Lee").

The Office Action asserts that the '108 patent teaches all the features of claim 5 except for one feature with respect to which Poon is cited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108 patent does not teach or suggest at least the following features that are presently recited in claim 5 by incorporation from independent claim 1:

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas; and

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer.

The Office Action asserts that the '108 patent teaches all the features of claim 8 except for one feature with respect to which the '108 patent is cited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108

patent does not teach or suggest at least the following features that are presently recited in claim 8 by incorporation from independent claim 7:

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas; and

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer.

The Office Action asserts that the '108 patent teaches all the features of claims 9, 10, 12, and 13 except for the etch rates recited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108 patent does not teach or suggest at least the following features that are presently recited in claims 9, 10, 12, and 13 by incorporation from independent claim 7:

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from

said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas; and

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer.

Furthermore, the '108 patent does not teach or suggest the selectivity rates as recited in the pending claims. The '108 patent discloses the formation of polishing mask 44' and oxide region 66' by polishing oxide region 66 and nitride layer 44, but it is silent as to any selectivity rate. *See* the '108 patent, Fig. 3L, col. 5, *ll.* 40-46. The '108 patent does not provide any teaching or suggestion to support the statement in the Office Action to the effect that the cited reference disclosure includes the selectivity rates that are recited in the pending claims.

The Office Action asserts that the '108 patent teaches all the features of claim 14 except for one feature with respect to which Poon is cited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108 patent does not teach or suggest at least the following features that are presently recited in claim 14 and in claims 15-17 by incorporation from independent claim 14:

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said

first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas; and

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second silicon dioxide layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and said silicon nitride layer.

Furthermore, Poon does not teach or suggest forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and consequently Poon does not teach or disclose the presently claimed methods with the features recited in claim 16.

The Office Action asserts that the '108 patent teaches all the features of claim 35 except for one feature with respect to which Lee is cited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108 patent does not teach or suggest at least the following features that are presently recited in claim 35 and in claims 36-37 by incorporation form claim 35:

forming a plurality of isolation trenches [having] through the exposed oxide layer at said plurality of areas, wherein electrically insulative material extend[ing]s continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer; and

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer

The Office Action asserts that the '108 patent teaches all the features of claim 38 except for one feature with respect to which Lee is cited therein. Applicants respectfully submit that the '108 patent does not teach or suggest the presently claimed methods, and in particular the '108 patent does not teach or suggest at least the following features that are presently recited in claims 39 and 40 by incorporation from independent claim 38:

forming a plurality of isolation trenches through the oxide layer at said plurality of areas, wherein electrically insulative material extends continuously between and within said plurality of isolation trenches;

each said isolation trench having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer; and

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer.

Pending claims 18-27, 31-34, and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the '702 patent or over a combination of the '702 patent with at least one of Poon and Lee.

The Office Action asserts that the '072 patent teaches all the features of claims 18 and 19 and also all the features of dependent claims 20-23 except for features with respect to which Lee or a

combination of Lee and Poon are cited therein. Applicants respectfully submit that the '072 patent does not teach or suggest the presently claimed methods, and in particular that the '072 patent does not teach or suggest at least the following features presently recited in independent claim 18 and in its dependent claims 19-23 by incorporation:

rounding the top edges of each of said isolation trenches; and

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces ... wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches.

Furthermore, Poon does not teach or suggest, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate. Consequently Poon doe snot teach or suggest the presently claimed methods with the features recited in claim 23.

The Office Action asserts that the '072 patent teaches all the features of claim 24. Applicants respectfully submit that the '072 patent does not teach or suggest the presently claimed methods, and in particular that the '072 patent does not teach or suggest at least the following features presently recited in claim 24:

rounding the top edges of each of said isolation trenches; and

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches.

The Office Action asserts that the '072 patent teaches all the features of claim 25. Applicants respectfully submit that the '072 patent does not teach or suggest the presently claimed methods, and in particular that the '072 patent does not teach or suggest at least the following features presently recited in claim 25:

rounding the top edges of each of said isolation trenches;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

The Office Action asserts that the '072 patent teaches all the features of claims 26-27, except for the disclosure of the claimed selectivity rates. Applicants respectfully submit that the '072 patent does not teach or suggest the presently claimed methods, and in particular that the '072 patent does not teach or suggest at least the following features presently recited in claims 25-27:

rounding the top edges of each of said isolation trenches; and

planarizing the conformal third layer by an etch using an etch recipe that etches said first

dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches. Furthermore, the planar surface shown in the '072 patent, Fig. 3M, does not imply that this reference teaches or suggests the recited claim limitations concerning selectivity rates. This reference does not provide the teaching or suggestion to support the statement in the Office Action to the effect that the cited reference includes the recited selectivity rates.

The Office Action asserts that the '072 patent teaches all the features of claims 31-34, except for features with respect to which Lee or the combination of Lee and Poon are cited therein. Applicants respectfully submit that the '072 patent does not teach or suggest the presently claimed methods, and in particular that the '072 patent does not teach or suggest at least the following features presently recited in claims 31-34:

rounding the top edges of said isolation trenches; and

planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches.

Furthermore, the '072 patent does not teach or suggest forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. Consequently, the '072 patent does not teach or suggest the presently claimed methods with the features recited in claim 34.

The Office Action asserts that the '072 patent in view of Lee teaches all the features of claim 42. Applicants respectfully submit that this combination does not teach or suggest the presently claimed methods, and in particular that this combination does not teach or suggest at least the following features presently recited in claim 42:

rounding the top edges of said isolation trenches; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer.

Applicants note that Poon and/or Lee, even if they were combinable with either one of the '108 patent or the '072 patent, do not provide any basis that would overcome the lack of teachings established with respect to the disclosure in the '108 patent or the '072 patent. None of the claimed methods as a whole is taught or suggested by the art of record, which in addition does not provide any suggestion of reasonable likelihood of success of the claimed methods. Accordingly, it may not be asserted that the teachings provided by the '108 patent or the '072 patent combined with the additional references of record are sufficient for one of ordinary skill in the art to make the substitutions, combinations or other modifications that are necessary to arrive to the claimed methods.

Consequently, Applicants respectfully submit that the cited references do not support a *prima facie* case of obviousness regarding the present claims. Applicants respectfully request the reconsideration and withdrawal of this rejection.

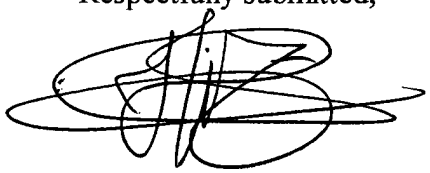
3. CONCLUSIONS

In view of the above, Applicants respectfully maintain that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 14th day of February 2002.

Respectfully submitted,



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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Applicant submits the following marked up version only for claims being changed by the current amendment, wherein the markings, if any, are shown by brackets (for deleted matter) and/or underlining (for added matter).

1. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

7. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing with a single etch recipe the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

said planarizing is performed in the absence of masking the conformal layer over each said isolation trench;

material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

14. (Thrice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of [said] each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and extending from an interface thereof with

said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second silicon dioxide layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and said silicon nitride layer; and

selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches, and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench.

18. (Twice Amended) A method of [a] forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

21. (Once Amended) A method according to Claim 18 , further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench, said liner being confined within each said isolation trench and [that] extend[s]ing from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically conductive material.

24. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

26. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

31. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edges of said isolation trenches;

filling each said isolation trench with a conformal second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap in each said isolation trench and extending over said spacers and over said silicon nitride layer; and

planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

34. (Once Amended) A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate; and

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

35. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

selectively removing said first layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches [having] through the exposed oxide layer at said plurality of areas, wherein electrically insulative material extend[ing]s continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

38. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

selectively removing said first layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches [having] through the oxide layer at said plurality of areas, wherein electrically insulative material extend[ing]s continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper

surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

42. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top

edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is curved;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

rounding the top edges of said isolation trenches; /

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trenches and extending over said spacers and over said first layer; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Four Times Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer

of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of leaving no gap within each said isolation trenches and extending over said spacers and over said first layer; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches, and wherein the microelectronic structure is defined at least in

part by the active area, the conformal second layer, and the first and second isolation trenches.

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